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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/597,017	07/06/2006	Olaf Such	PHDE040009US	4785

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
BRYANT, MICHAEL C	

ART UNIT	PAPER NUMBER
2884	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/597,017	SUCH ET AL.	
	Examiner	Art Unit	
	Casey Bryant	2884	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Applicant's reply, filed 10/12/2007, has been received and entered. Claims 1 and 4-6 have been amended. Claim 3 has been cancelled. Claims 10-21 have been added. Thus, claims 1, 2, and 4-21 remain currently pending in this application.

Response to Arguments

2. Applicant's arguments filed 12/12/2007 have been fully considered but they are not persuasive. On page 6 of the reply, the Applicant states that independent claim 1 has been amended to include aspects of claim 3 and that no new matter has been added. While the Examiner agrees that aspects of claim 3 have been incorporated into independent claim 1, inclusion of the phrase "reside on a same CMOS semiconductor structure" distinguishes the claimed subject matter from previously submitted claim 3 in that two elements are both located on a semiconductor structure does not necessarily require that to be the same semiconductor structure. In view of the new subject matter and the added new claims 10-21, a new search is required.

Claim Rejections – 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Rocha et al. (ROCHA, J.G., et al, CMOS X-ray Image Sensor with Pixel Level A/D Conversion. IEEE European Solid-State Circuits Conference. (2003), p. 121-124).

With respect to claim 1, Rocha teaches a detector having a plurality of elements, each of the plurality of elements including an integrated differential SD modulator and wherein the element and the corresponding integrated SD modulator reside on a same CMOS semiconductor structure (on-chip)(Figure 3; p. 121, column 2; p. 122, column 1; p. 123, column 1).

With respect to claim 2, Rocha teaches the SD modulator extended with a decimation filter (p. 124, column 1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 4 and 6-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boles et al. (BOLES, Colby D., Colby D., Bernhard E. Boser, Bruce H. Hasagawa, and Joseph A. Heanue. "A Multimode Digital Detector Readout for Solid-State medical Imaging Detectors." IEEE Journal for Solid State Circuits 33, No. 5 (1998)), in view of Rocha.

With respect to claim 1, Boles teaches a detector having a plurality of elements, each of the plurality of detection elements including an integrated differential SD modulator (abstract; II, A, para. 1; Figure 9), but does not specifically describe the plurality of detection elements and the corresponding integrated SD modulators residing on the same CMOS semiconductor substrate. Rocha teaches a detector wherein the pixels and a SD modulator reside on a same CMOS semiconductor structure (Figure 3; p. 121, column 2; p. 122, column 1; p. 123, column 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify

the detection elements and SD modulators of Boles as located on the same CMOS structure, as taught by Rocha, in order to reduce manufacturing costs and improve compactness of the electronics (p. 121, column 2).

With respect to claim 2, Boles discloses the SD modulator as having a decimation filter (Figure 1; II, A, 2).

With respect to claim 4, Boles discloses each SD modulator having a current feedback on the signal of a pixel with a switch capacitor (SC) source (Part C, para. 1).

With respect to claim 6, although Boles does not specifically disclose the comparator as an auto-zero comparator, it would have been obvious to one of ordinary skill in the art at the time of the invention to specify the comparator as auto-zeroing in order to reset the component to start at a known state (III, B, 3).

With respect to claim 7, Boles teaches a semiconductor image sensor (I, para. 4).

With respect to claim 8, Boles teaches an x-ray detector (I, para. 4).

With respect to claim 9, Boles teaches a CT x-ray device (I, para. 1).

With respect to claim 10, Boles teaches a radiation sensitive detector array comprising a photosensor and a Sigma Delta Analog-to-Digital (SD A/D) component (Figure 1; I, para. 3) as located on the same chip (Intro, para. 3), but fails to specifically teach the photosensor and the SD A/D component as located on the same substrate. But as suggested by Boles, it is known to locate A/D converter electronics and detection elements on the same substrate, as taught by Rocha (Figures 2&3; 2 "Sensor description"). It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify the photosensor and the SD A/D component on the same substrate, as taught by Rocha, in order to reduce the manufacturing cost. Furthermore, it has been held that integrating parts previously known without producing any new and unexpected result involves only routine skill in the art. *In re Larson 340 F.2d 965 144 USPQ 347 (CCPA 1965).*

With respect to claim 11, Boles teaches the SD A/D component including an integrator bank and a comparator (Figure 9; III, B., columns 1 and 2).

With respect to claim 12, Boles teaches the integrator bank including two integrators (Figure 9; III, B., 2).

With respect to claim 13, Boles describes the two integrators as capable of different orders (III, B., 2). It would have been obvious to one of ordinary skill in the art at the time of the invention to specify the integrators as different orders, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesh, 617 F.2d 272, USPQ 215 (CCPA 1980).*

With respect to claim 14, Boles teaches the SD A/D component signal sent to a decimation filter that produces a signal having a lower sampling rate and a higher dynamic range with respect to the output signal of the SD A/D component (II, A, 2; IV, B).

With respect to claims 15 and 16, neither Boles or Rocha teach the decimation filter providing a 17-bit signal output, but instead Boles discloses the decimation filter providing a 20-bit conversion signal output from the 1-bit output of the SD A/D component(II, A, 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify a 17-bit output, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesh, 617 F.2d 272, USPQ 215 (CCPA 1980).*

With respect to claims 17, 19 and 20, Boles teaches a method comprising detecting radiation with a photodetector, producing a first signal indicative of the detected radiation, wherein the first signal has a first dynamic range of 80dB (detector current: see Intro, para. 2), and generating a second signal based on the first signal with a sigma-delta a/d converter, wherein the second signal has a second dynamic range of greater than 120dB, and wherein the photodetector and sigma-delta a/d converter reside on the same chip (Table 1; Introduction).

With respect to claim 18, Boles teaches the first signal (detector) having a first sampling rate (2kHz) and the second signal (sigma-delta a/d converter) has a second sampling rate (2kHz)(Introduction; I, A). It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify a higher sample rate for the detector or a smaller sample rate for the a/d converter, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesh, 617 F.2d 272, USPQ 215 (CCPA 1980).*

With respect to claim 21, Boles teaches continuously integrating the first signal to generate the second signal (Figure 9; III, B, 2).

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boles in view of Rocha and Ribner (US 5142286).

With respect to claim 5, Boles and Rocha teach the device of claim 1 but fail to teach a cascaded arrangement of SD modulators in at least one of the detector elements. Ribner teaches the detector having a detection element with a cascaded SD modulator arrangement (Figures 3A-B)(column 12, line 30-column 13, line 46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Boles to specify the cascaded multi-stage SD modulator taught by Ribner in order to reduce interfering signal noise.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the

mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Casey Bryant whose telephone number is (571) 270-1282. The examiner can normally be reached on Monday - Friday, 8am - 5pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Porta can be reached on (571)272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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